

FIG. 2



FIG. 3
(PRIOR ART)

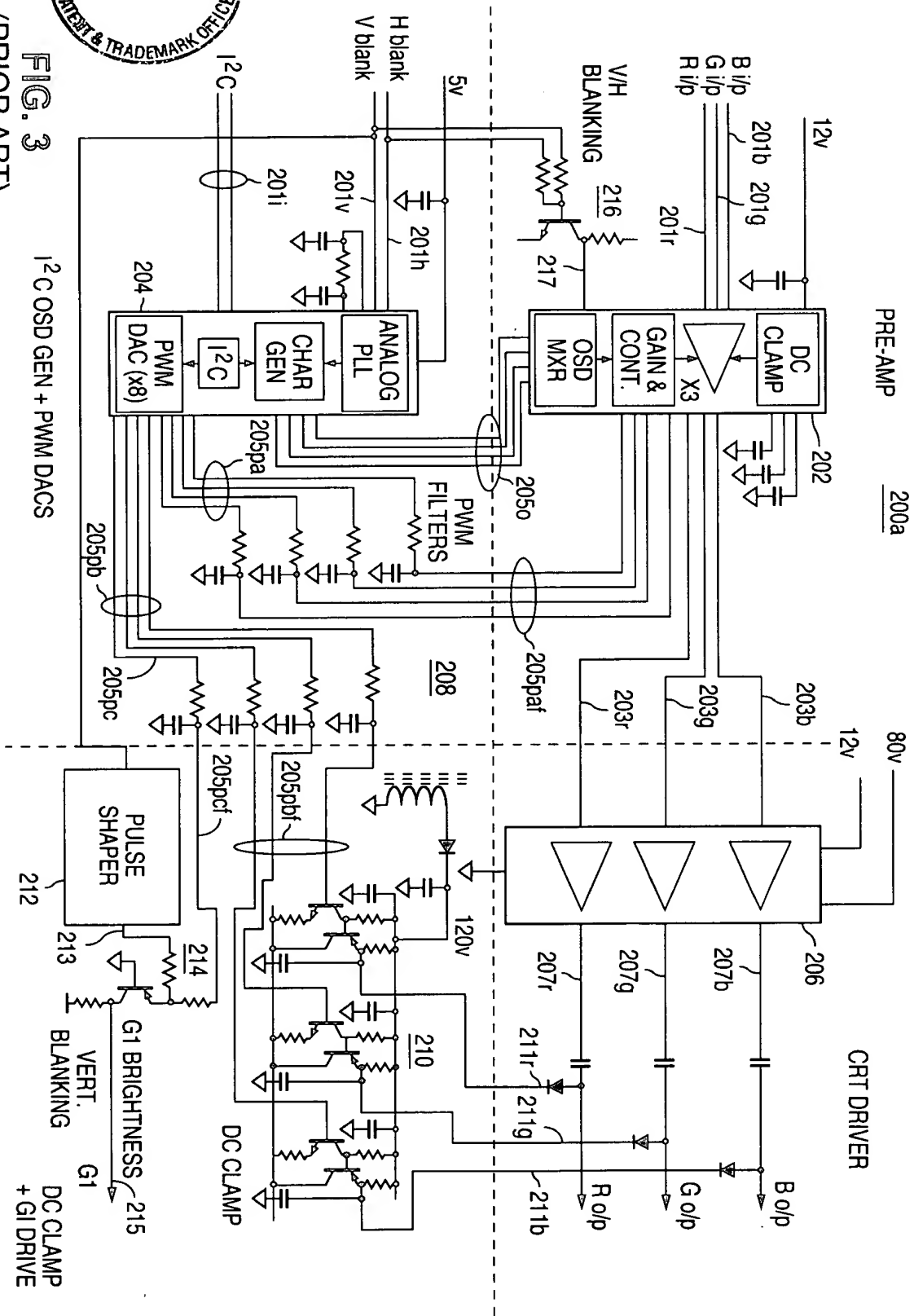
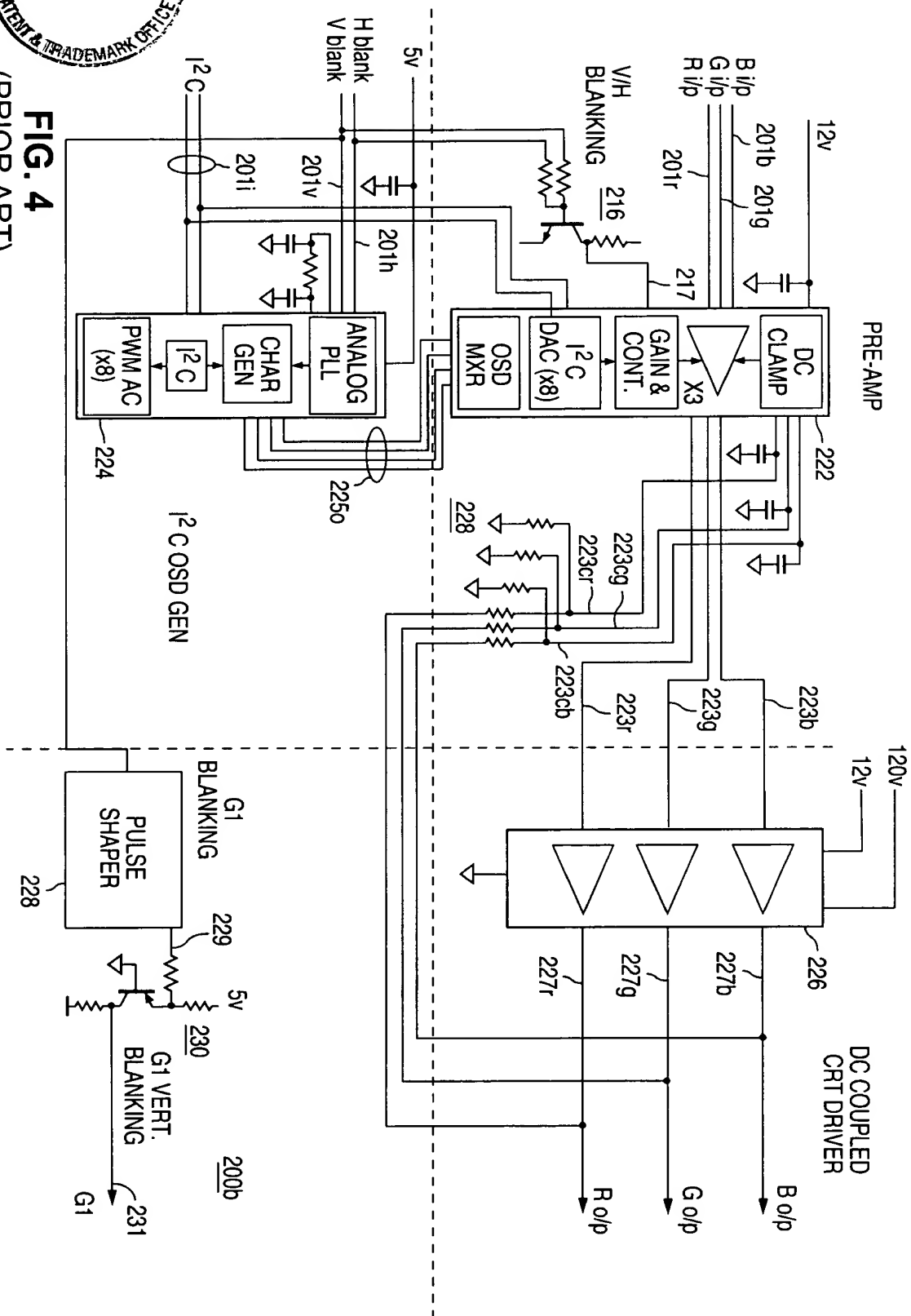
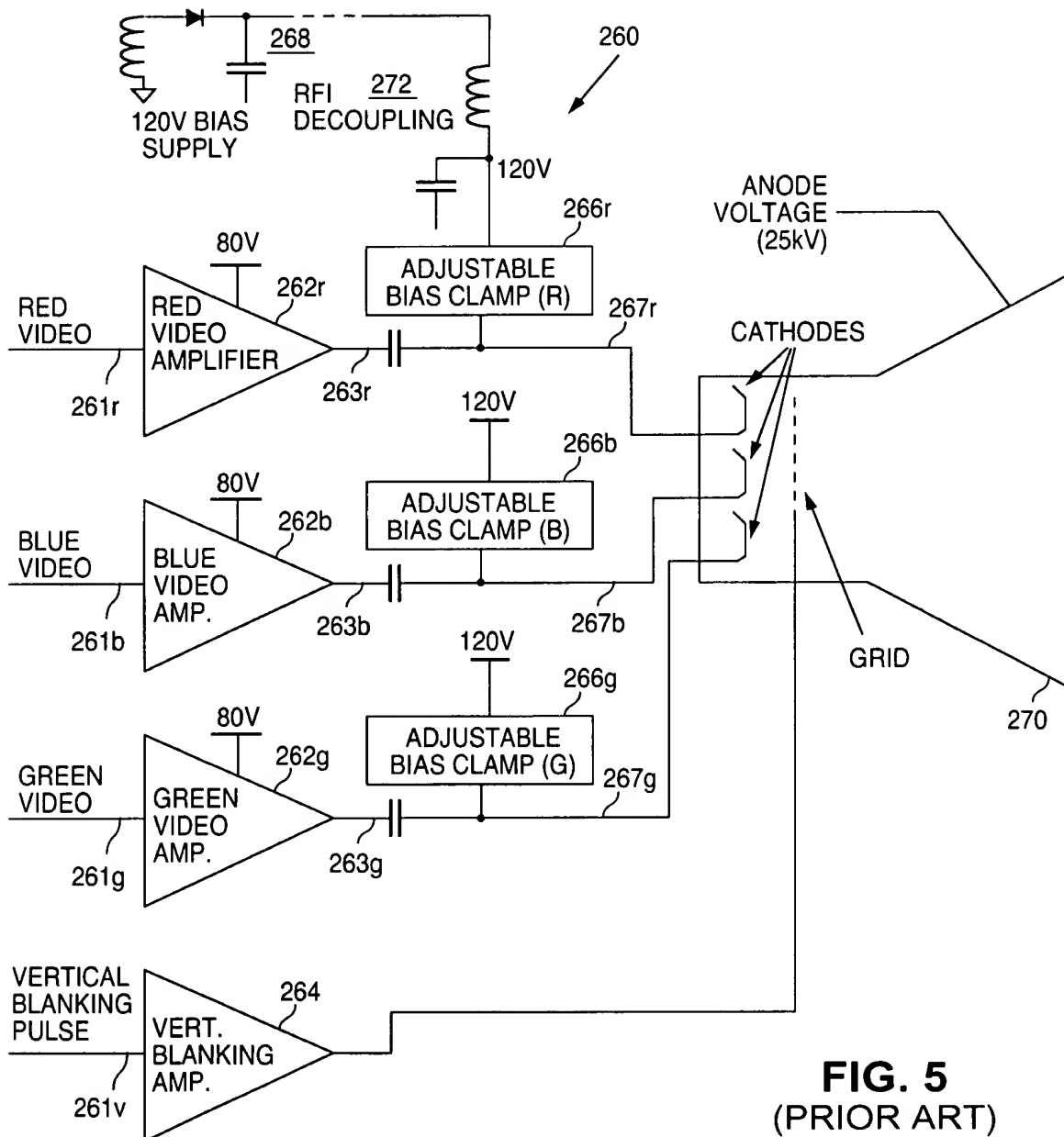




FIG. 4
(PRIOR ART)





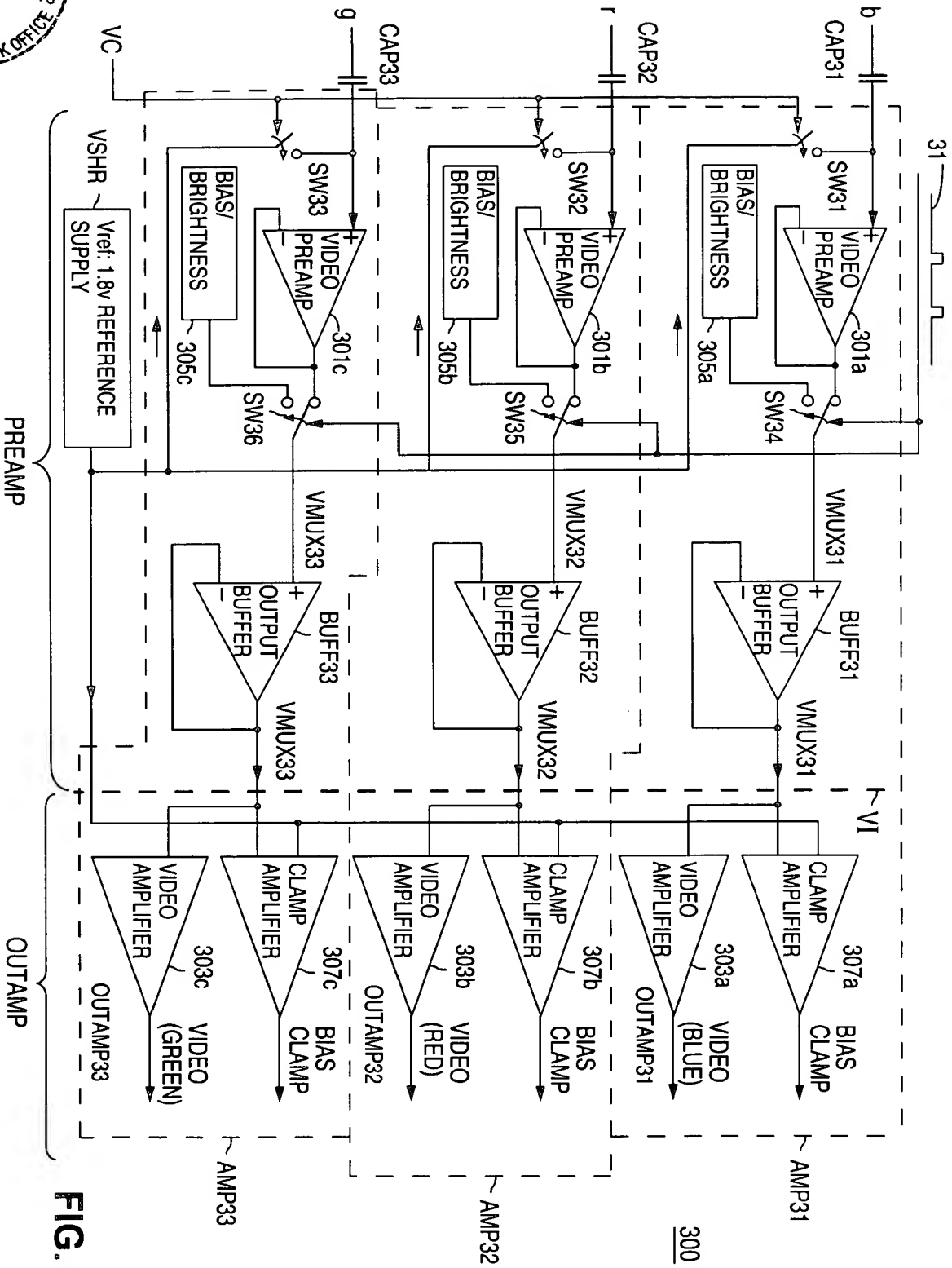


FIG. 6

FIG. 7

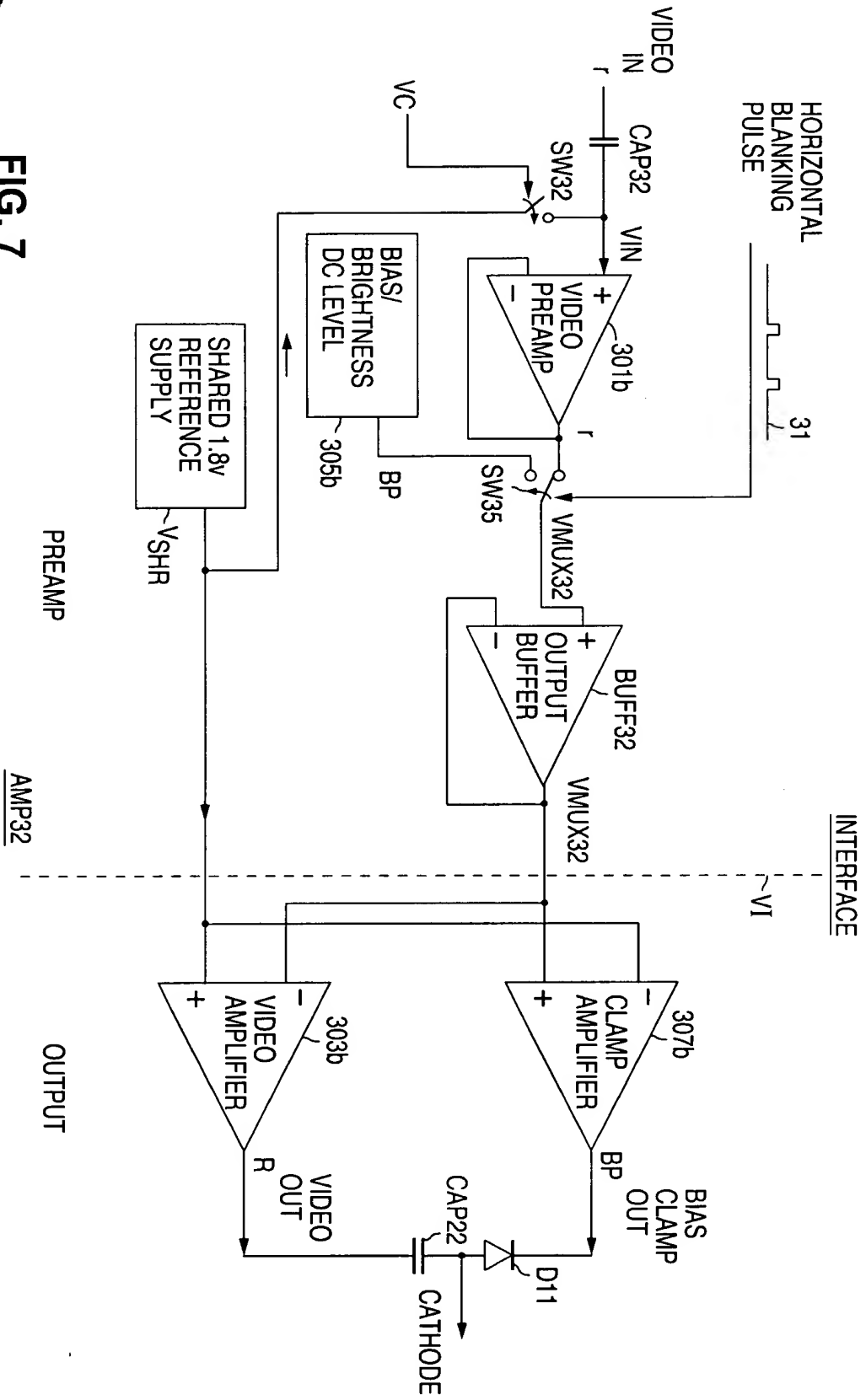


FIG. 8A

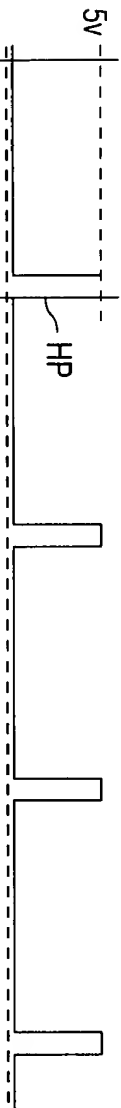


FIG. 8B

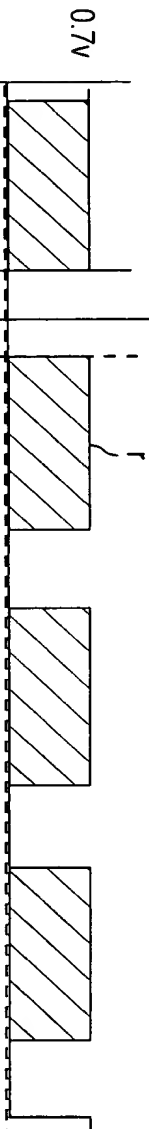


FIG. 8C

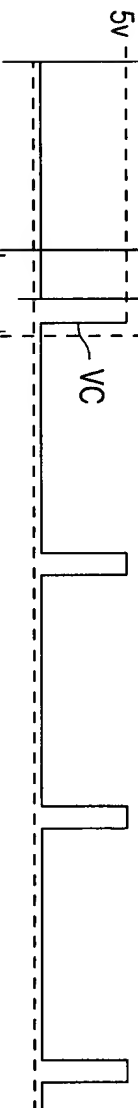


FIG. 8D

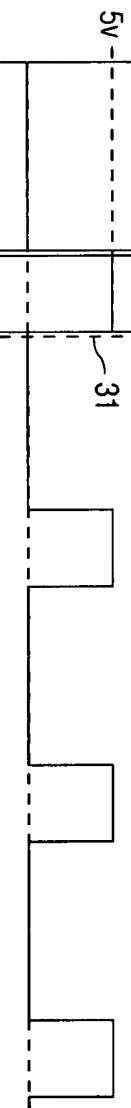
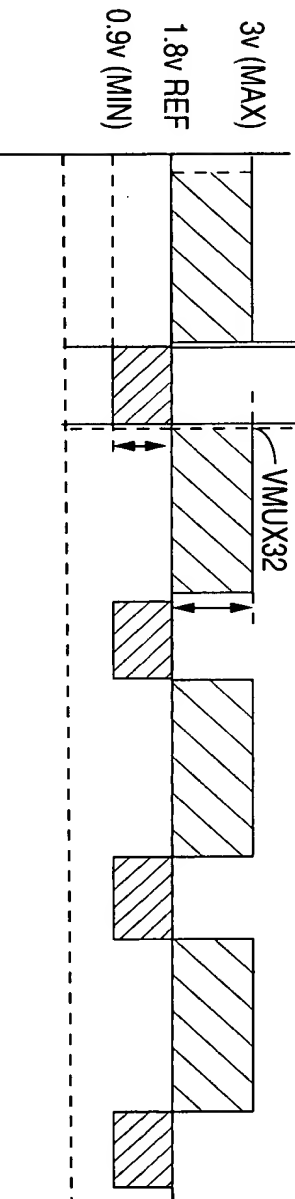


FIG. 8E



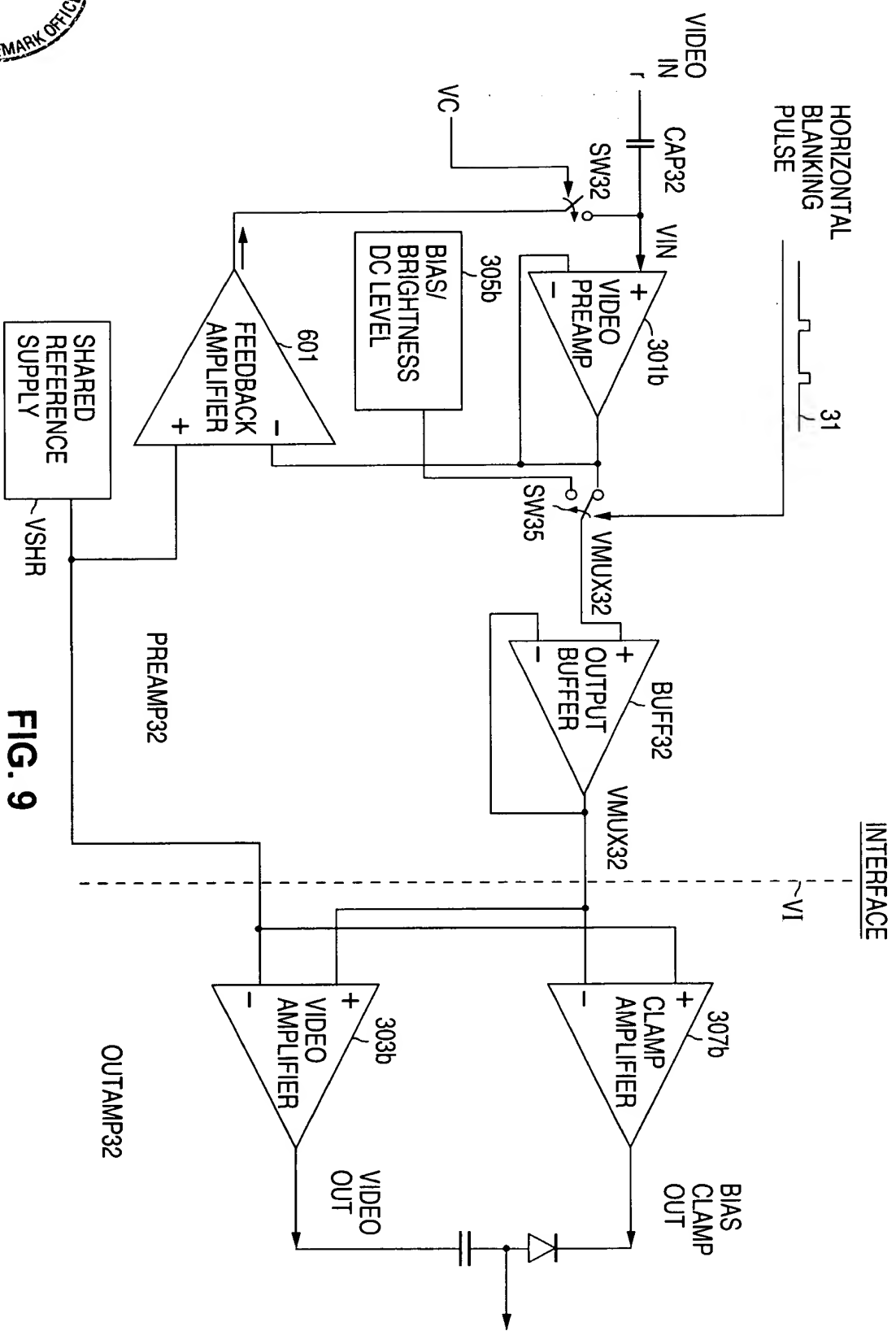


FIG. 9

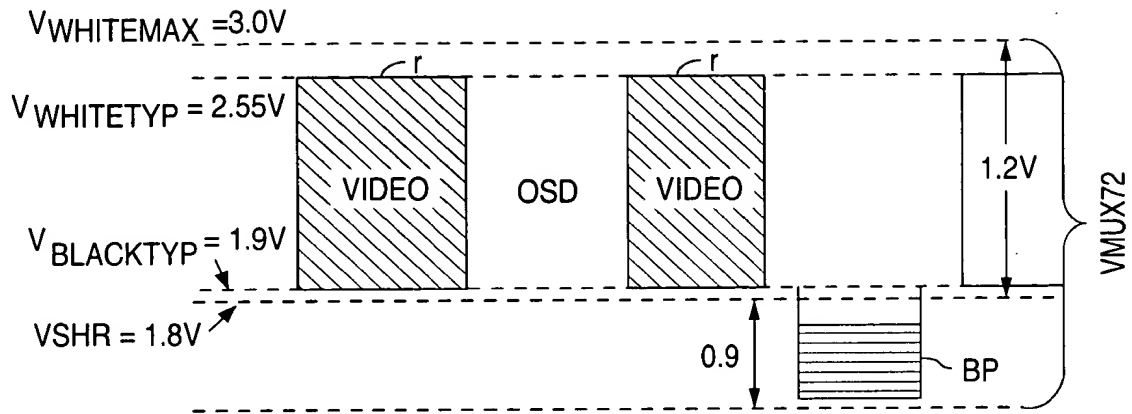


FIG. 10

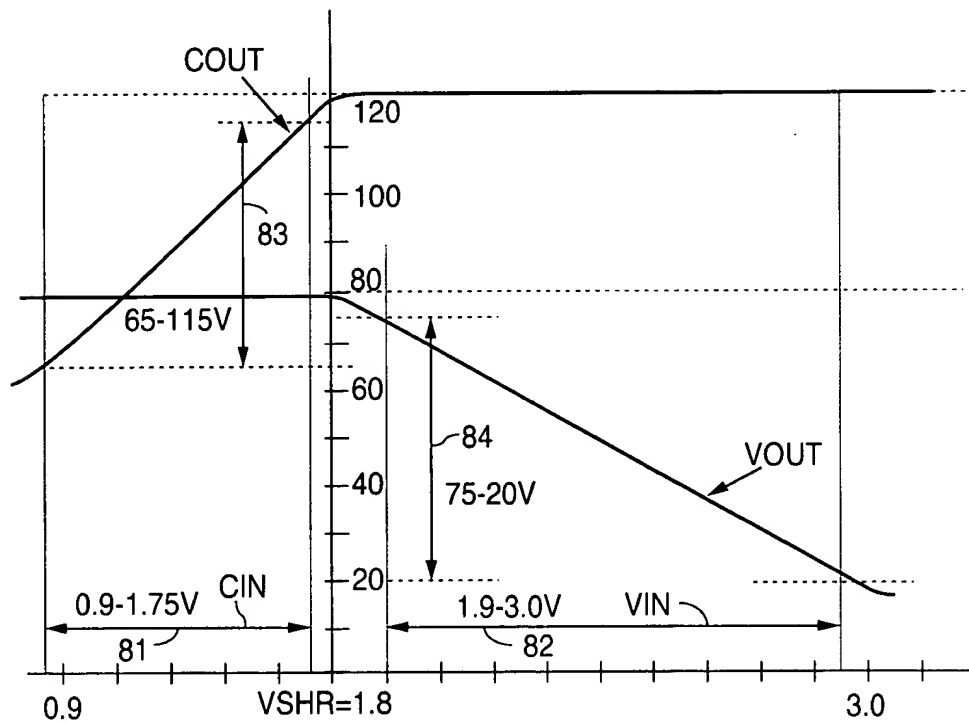
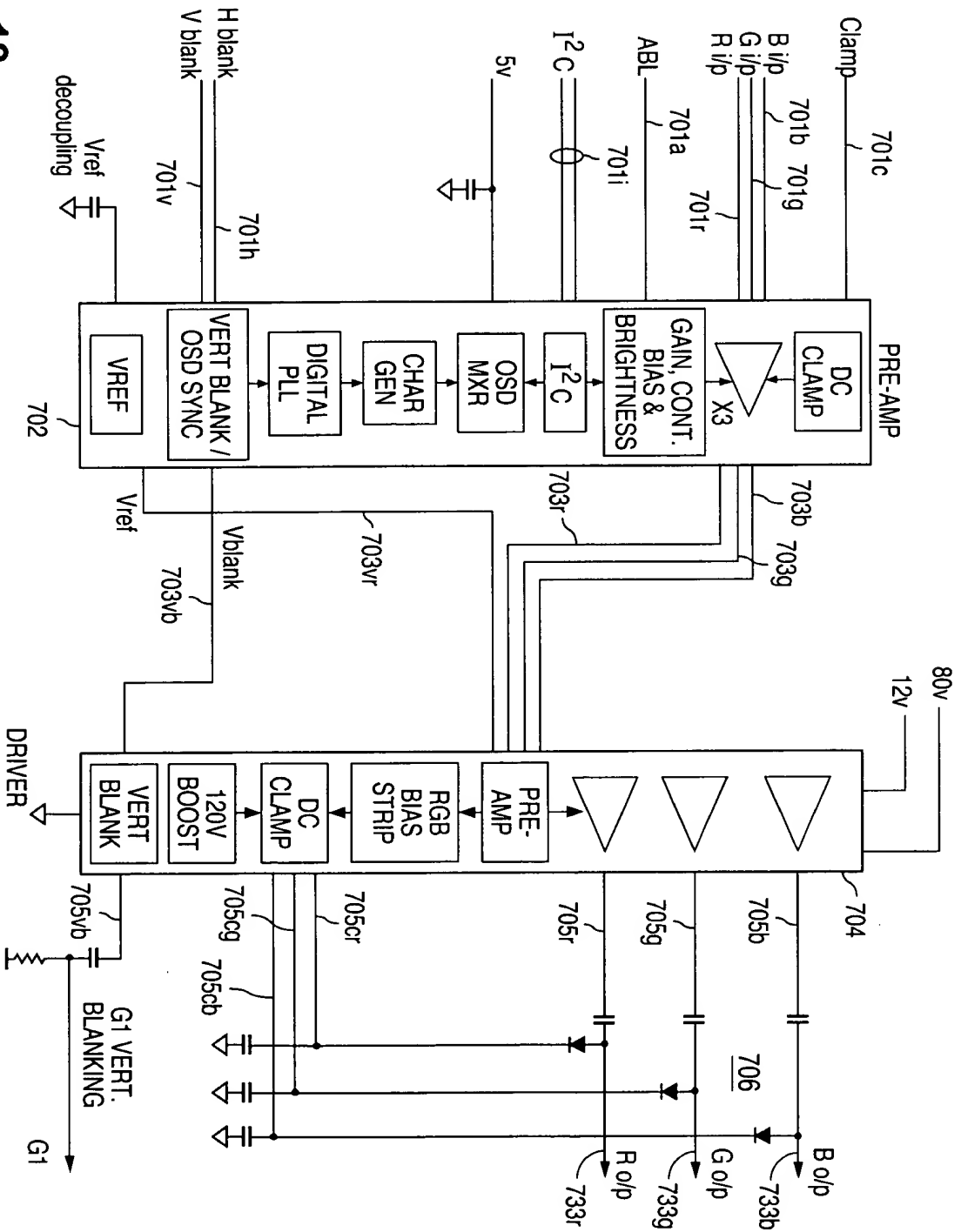


FIG. 11

FIG. 12



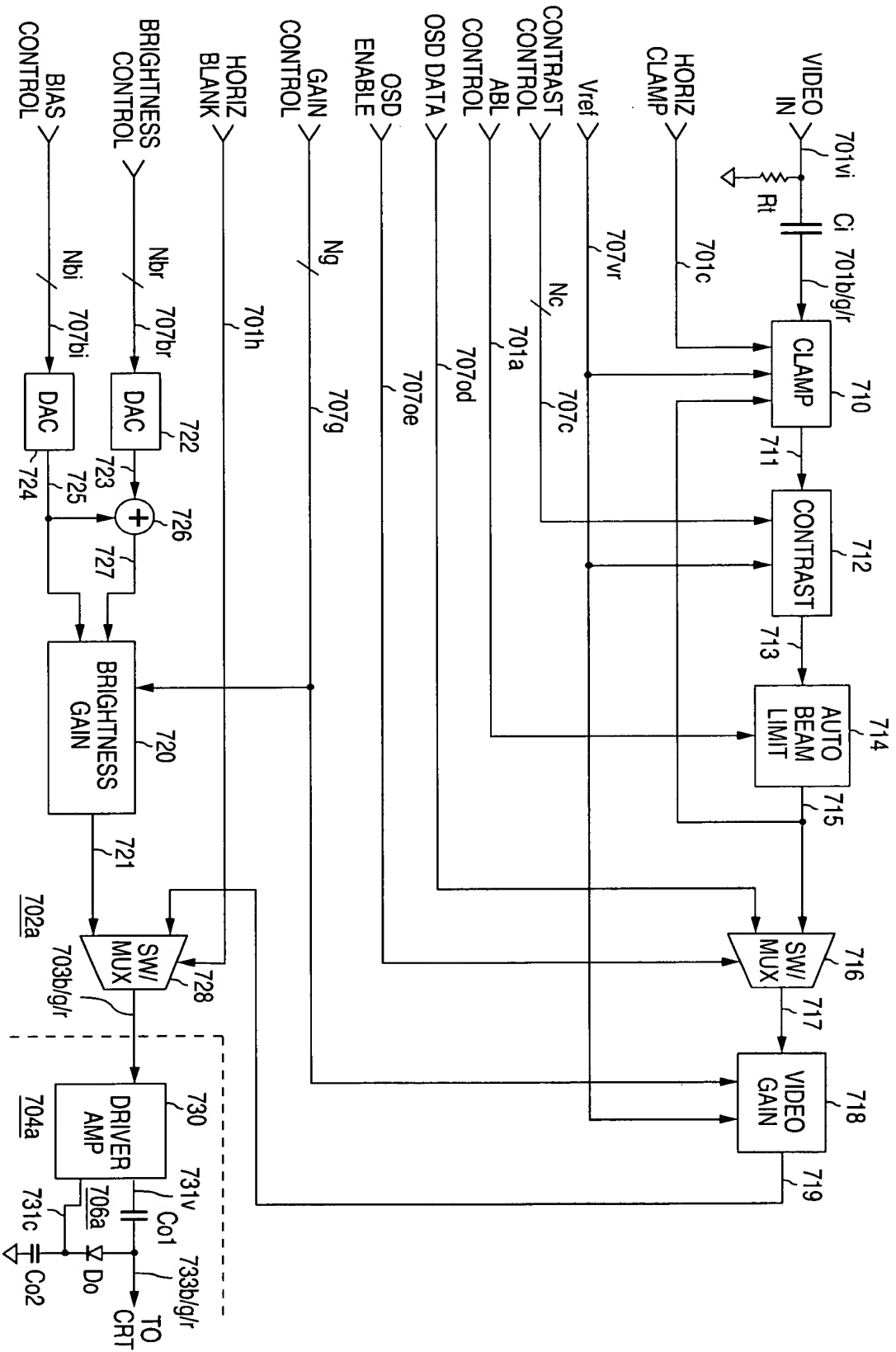
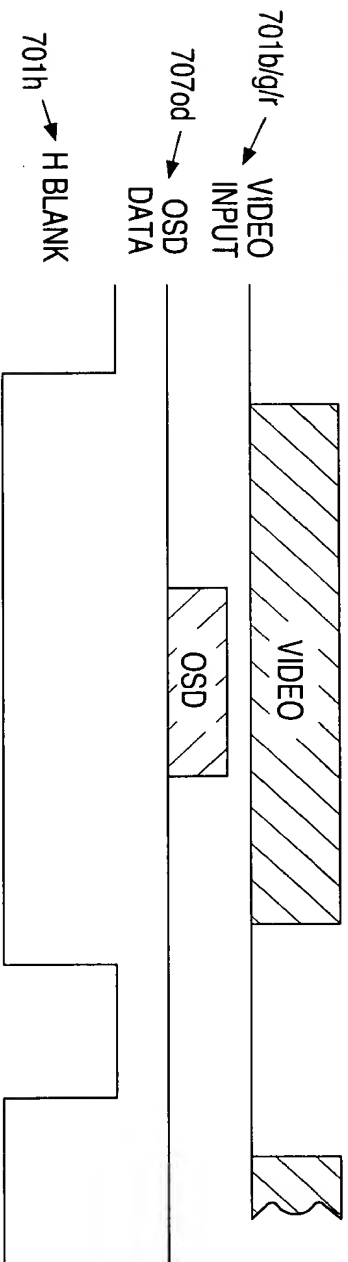


FIG. 13



INPUT SIGNALS



OUTPUT SIGNALS

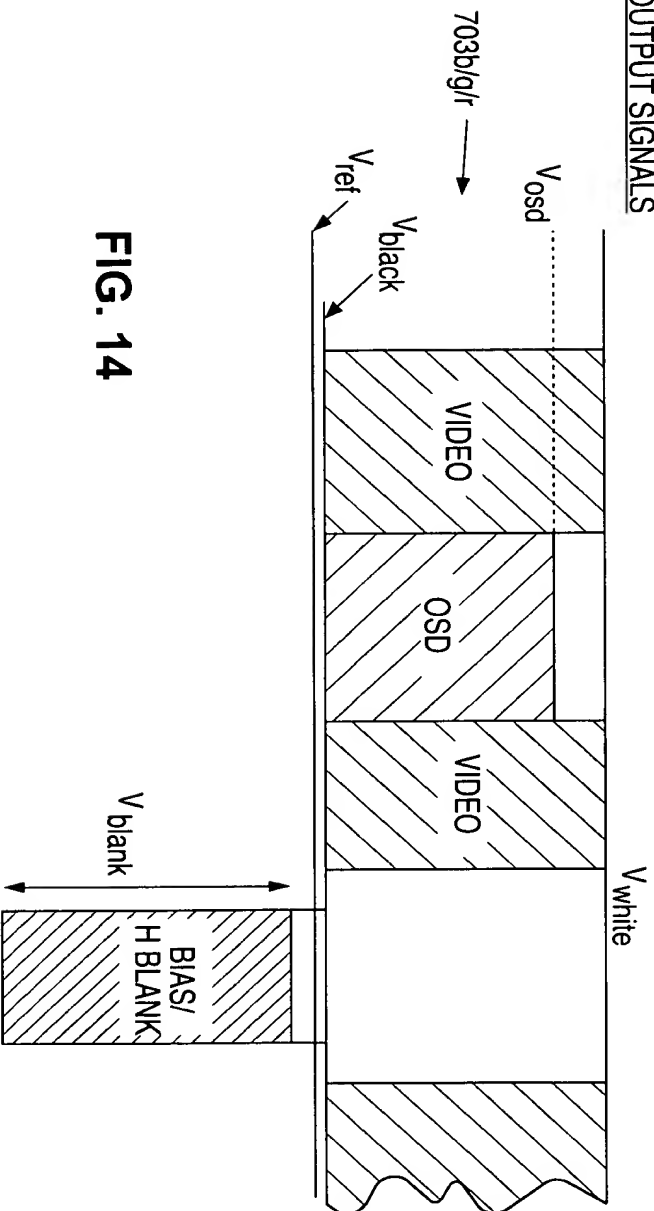


FIG. 14

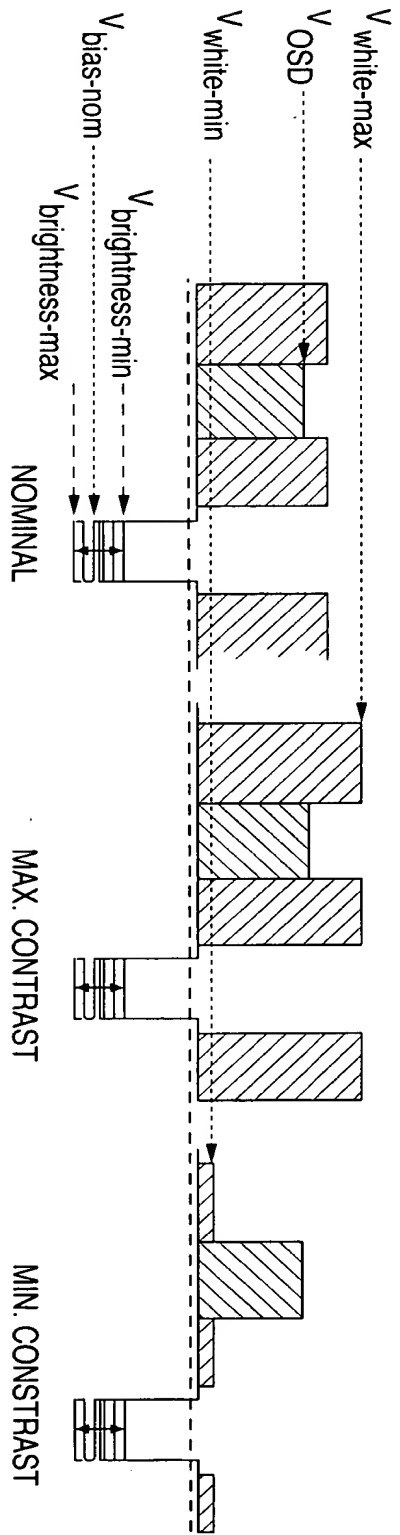


FIG. 15

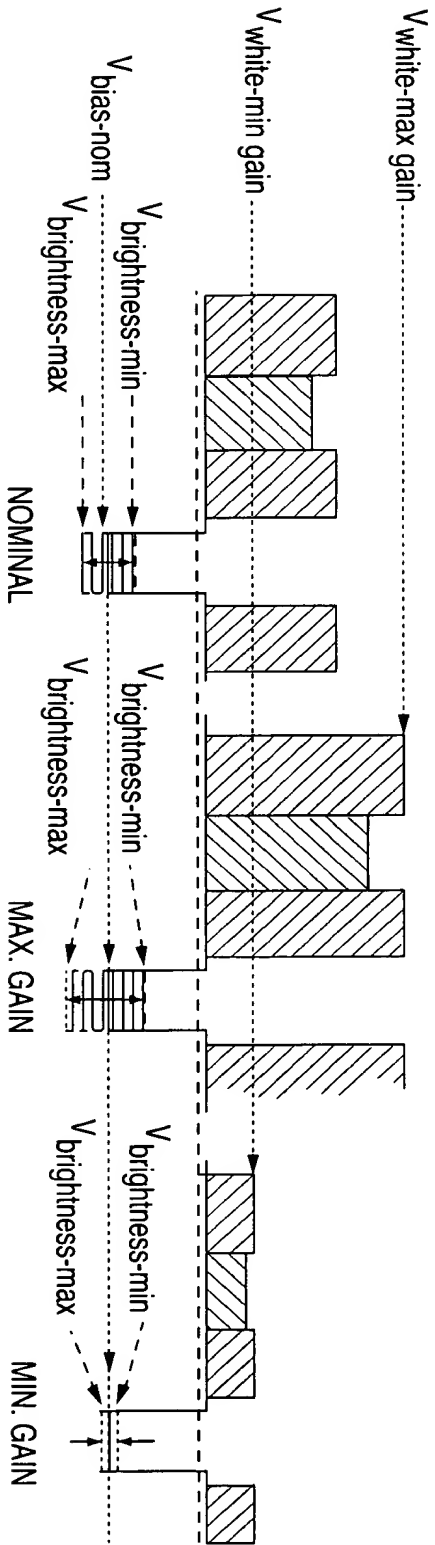


FIG. 16

FIG. 17

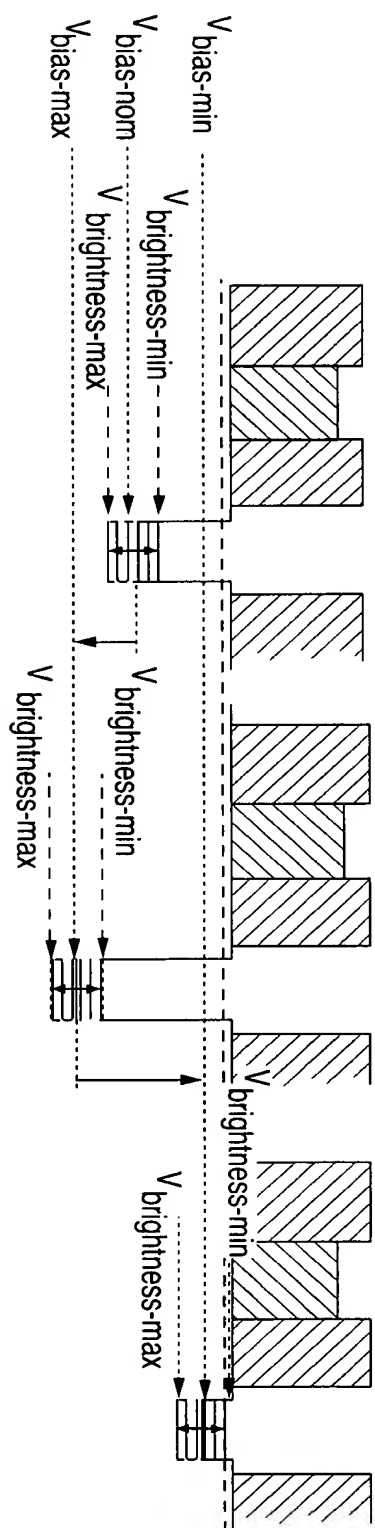
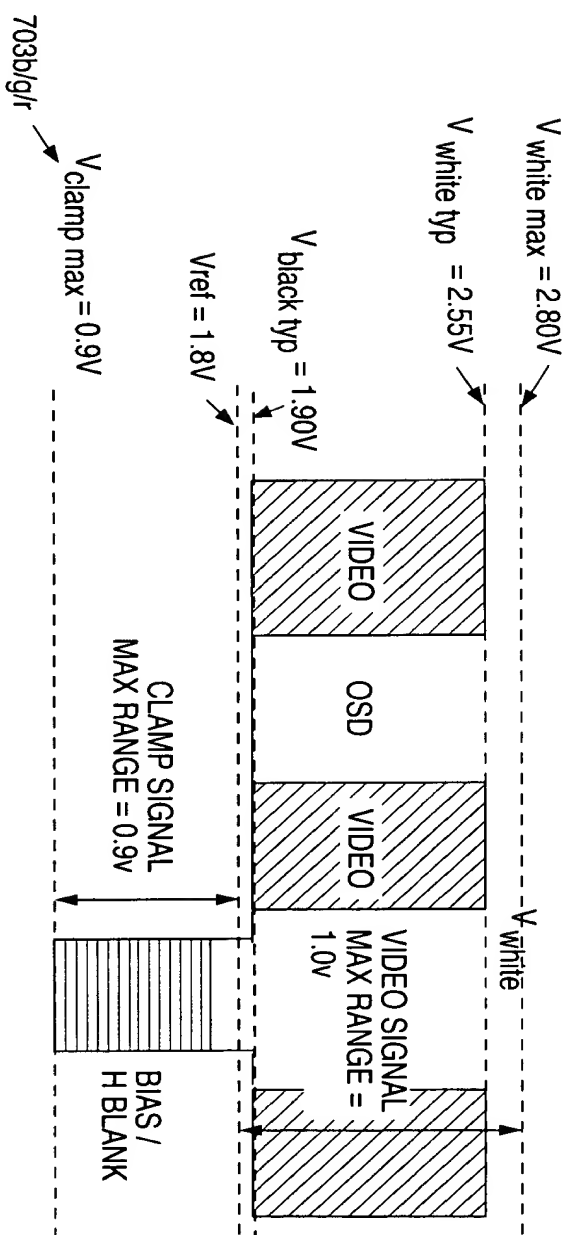


FIG. 18



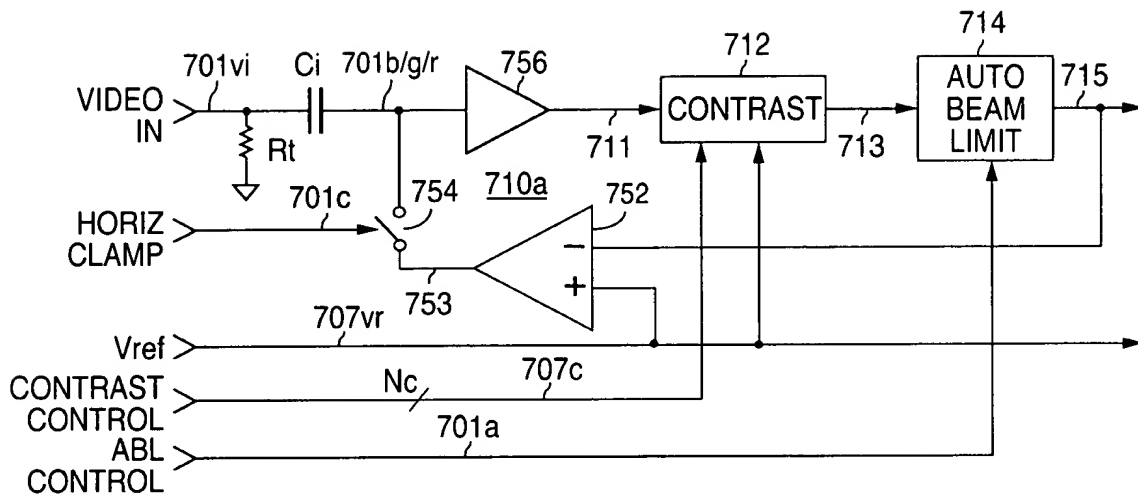


FIG. 19

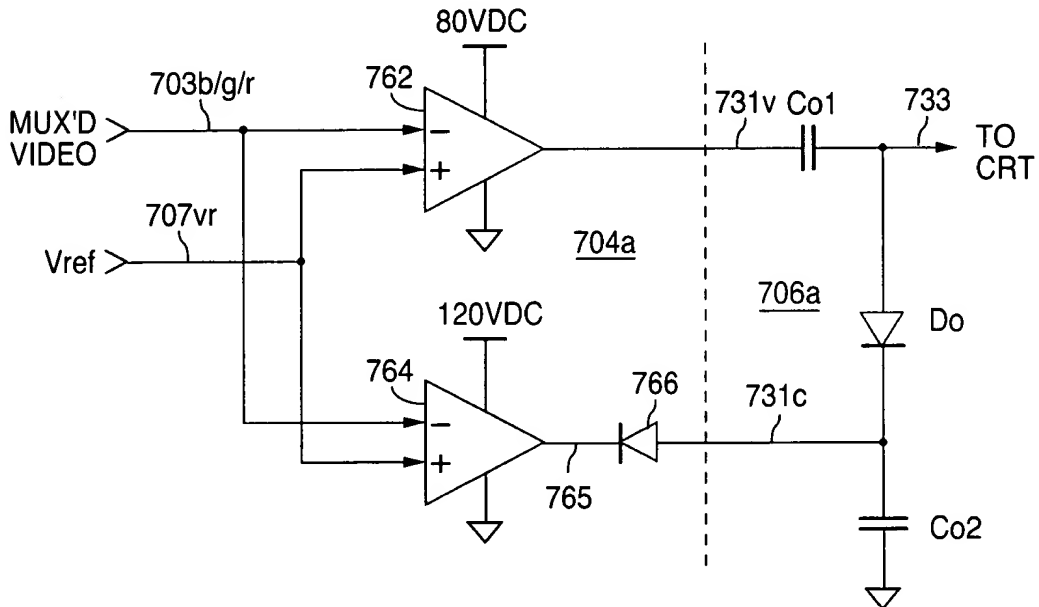


FIG. 20

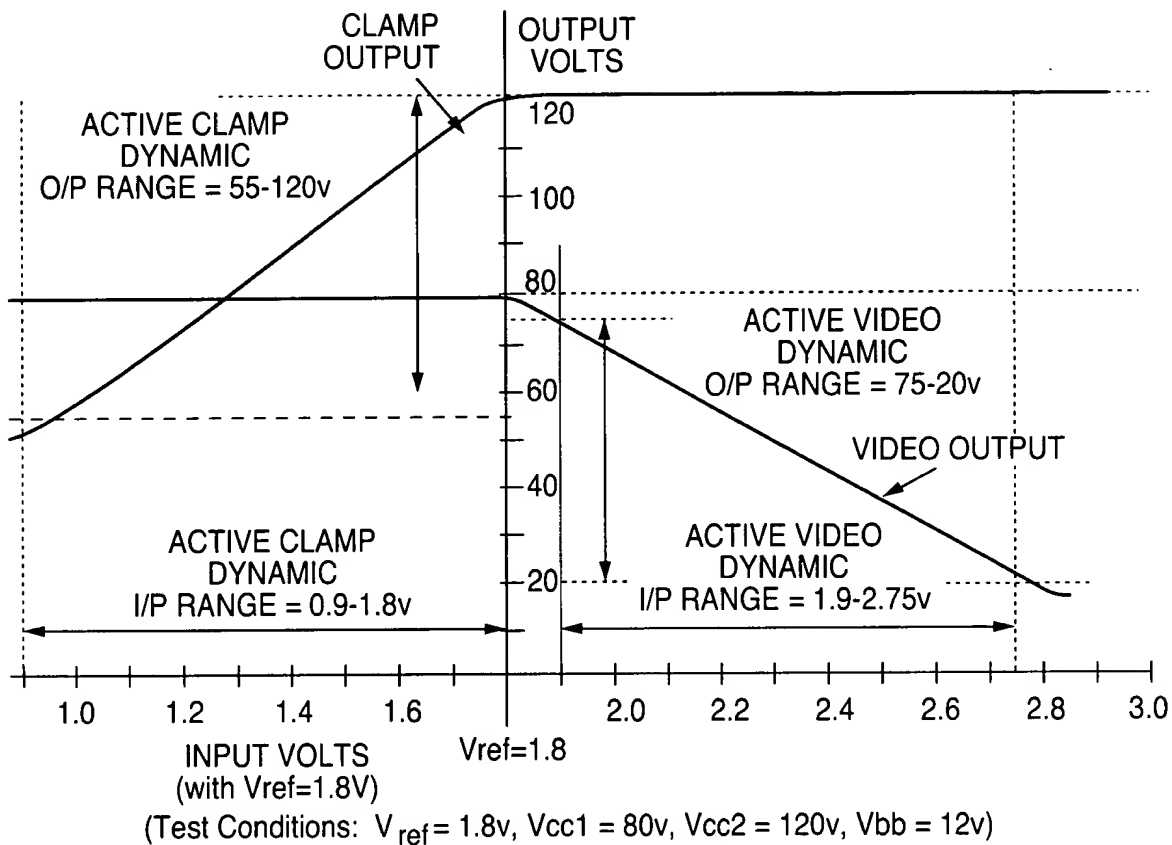


FIG. 21

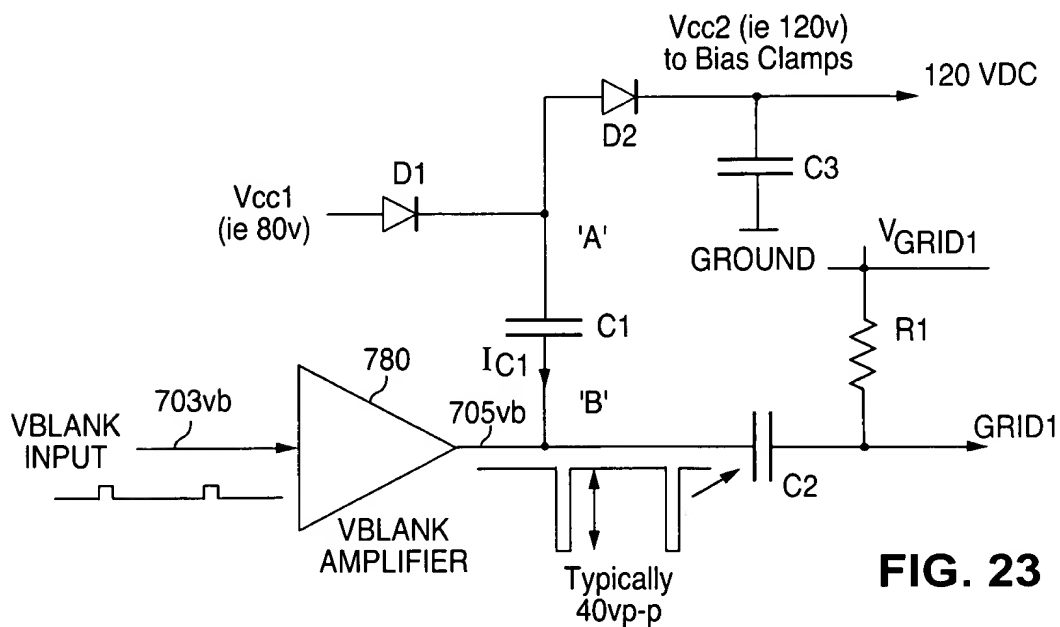


FIG. 23

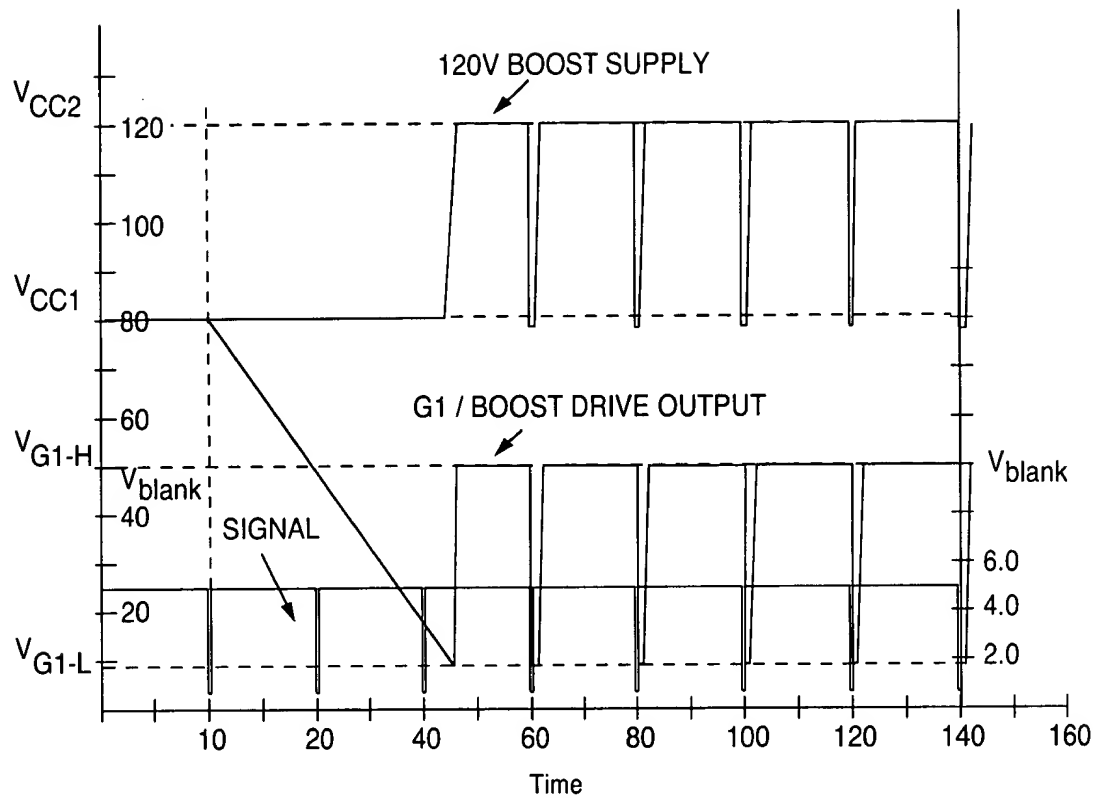


FIG. 22

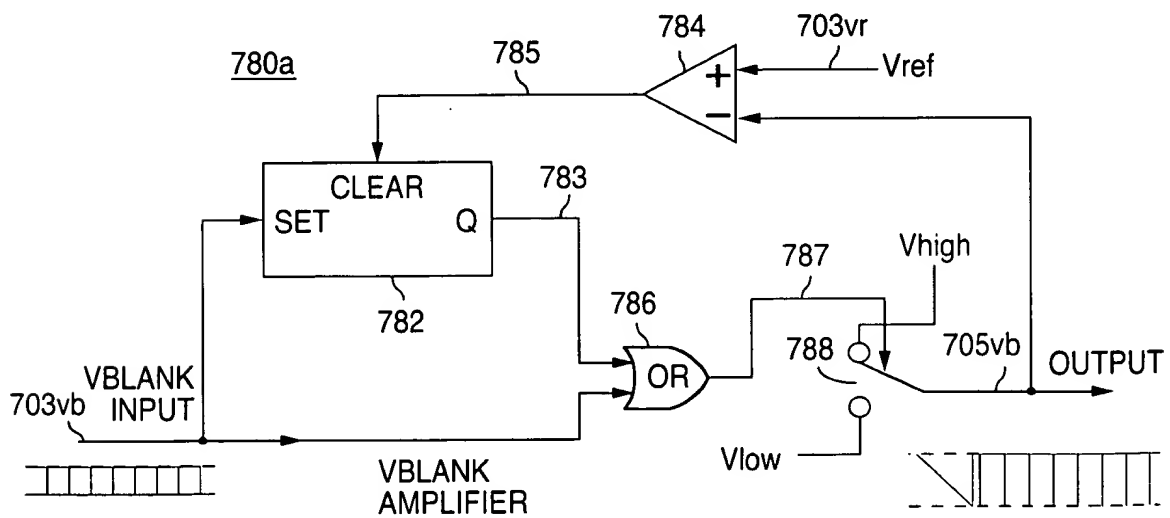


FIG. 25

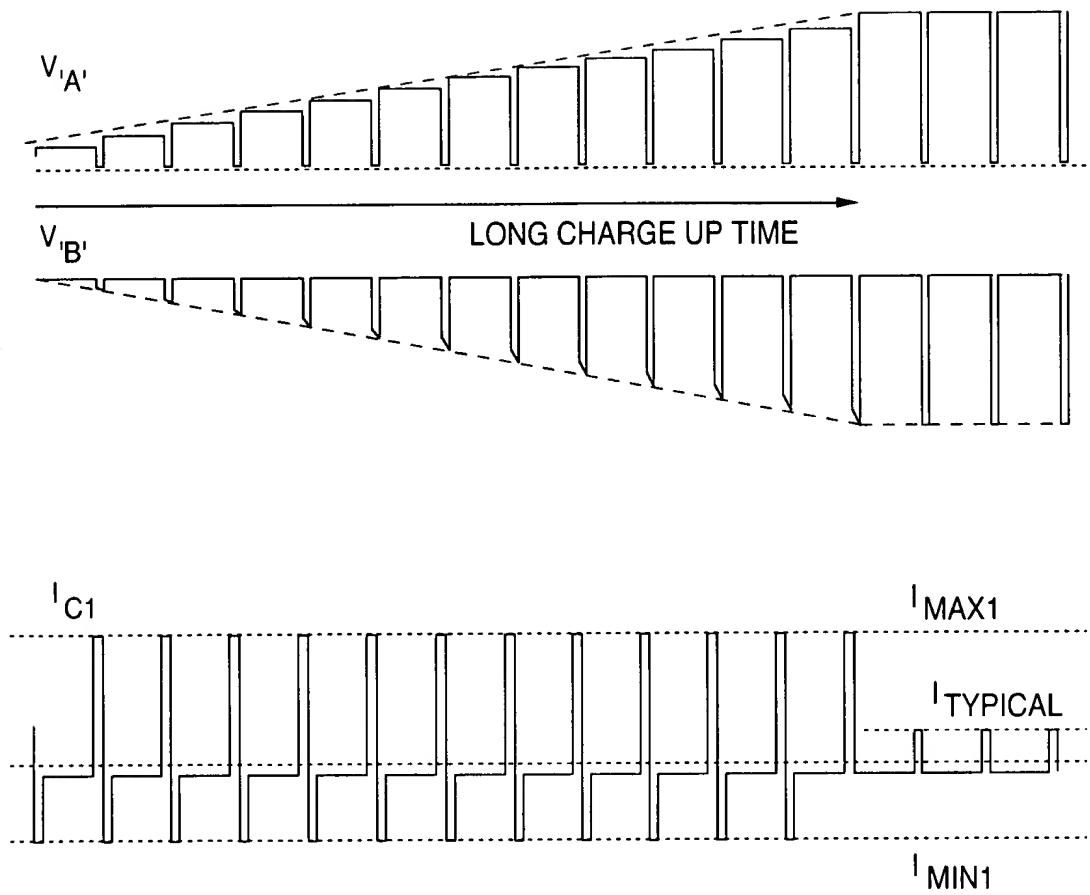


FIG. 24

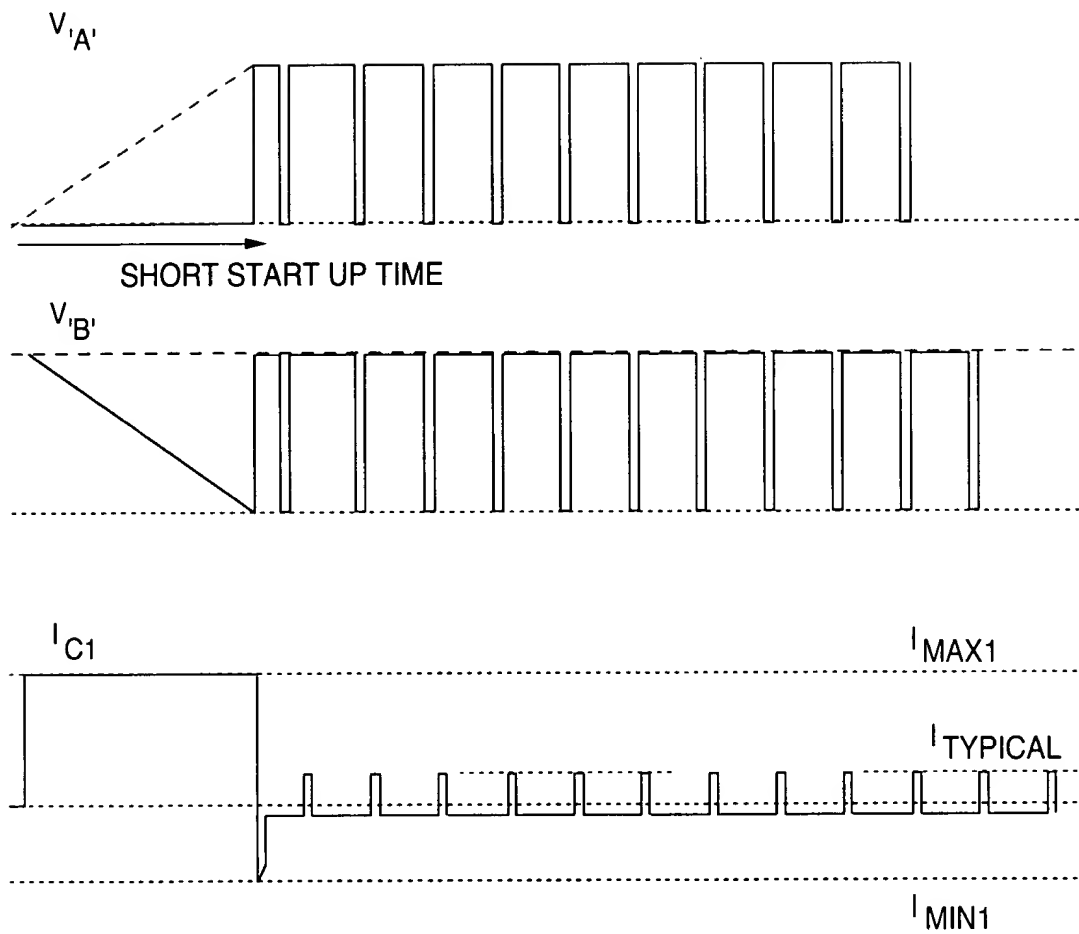


FIG. 26

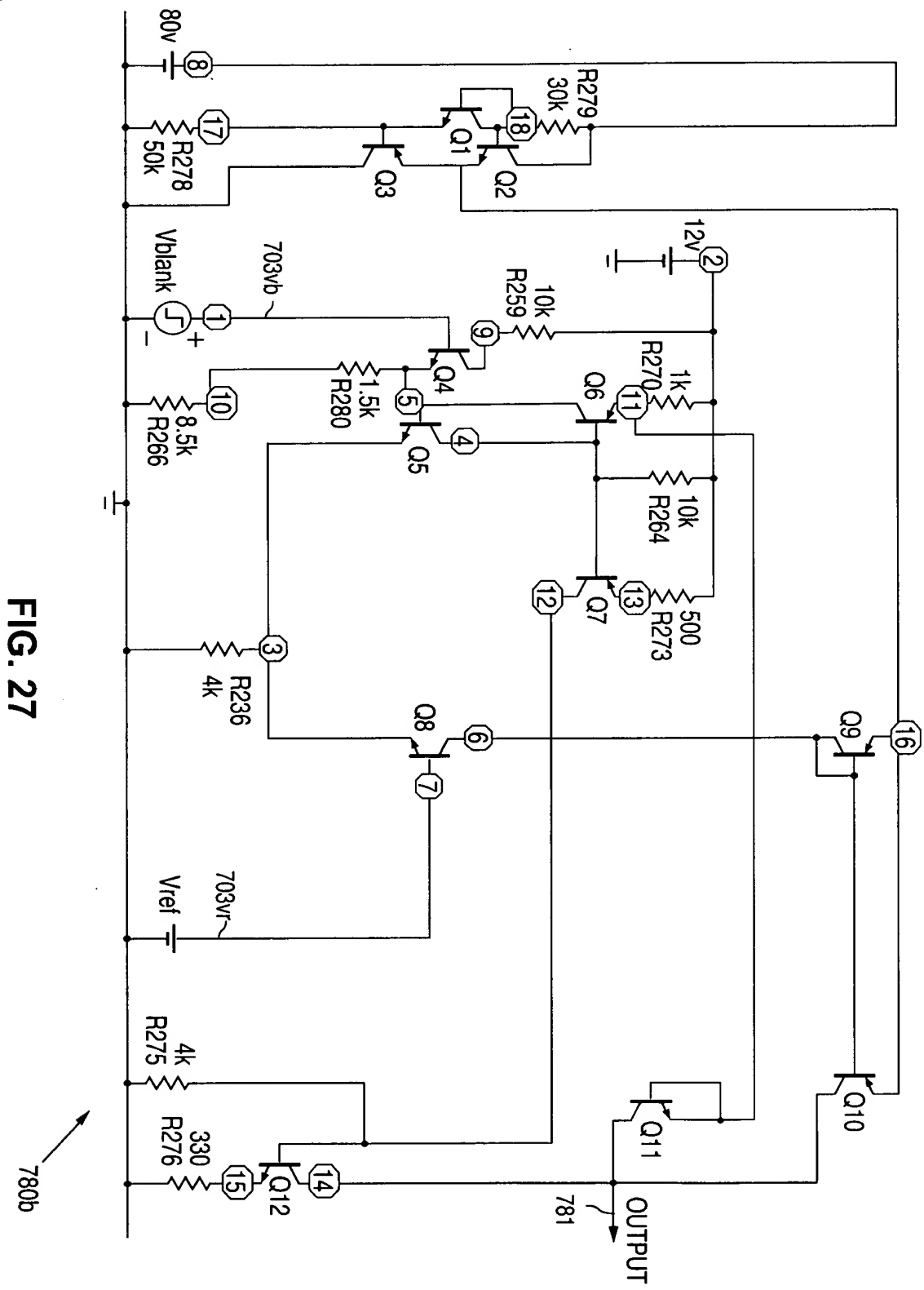


FIG. 27

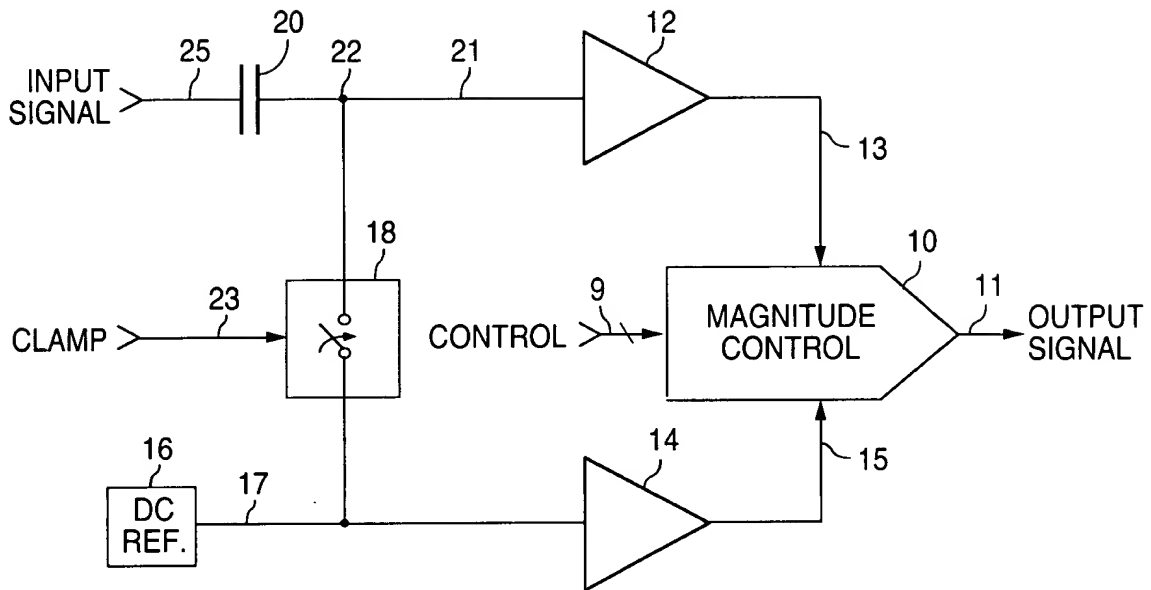


FIG. 28

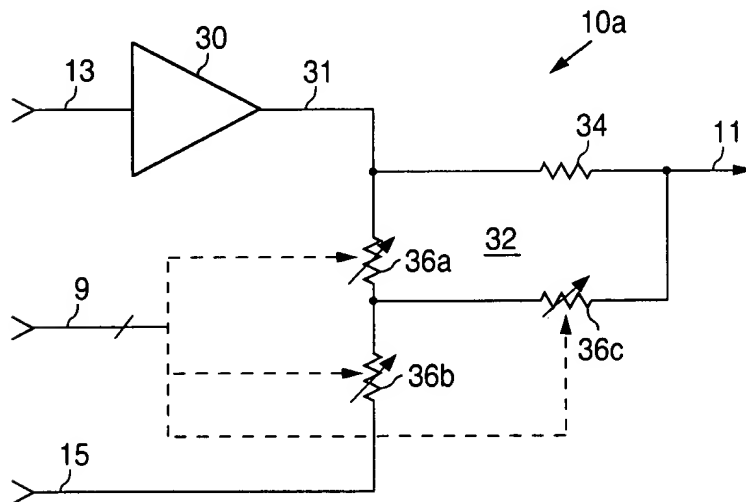


FIG. 29

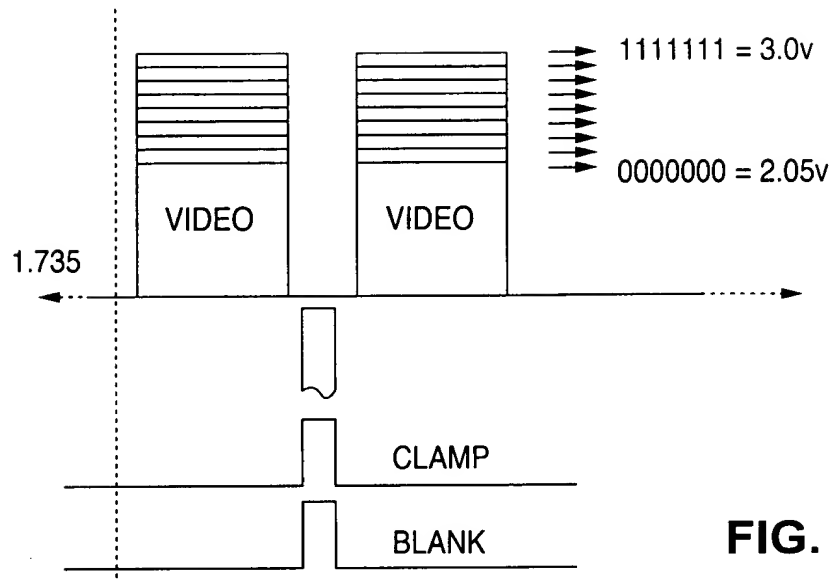


FIG. 30

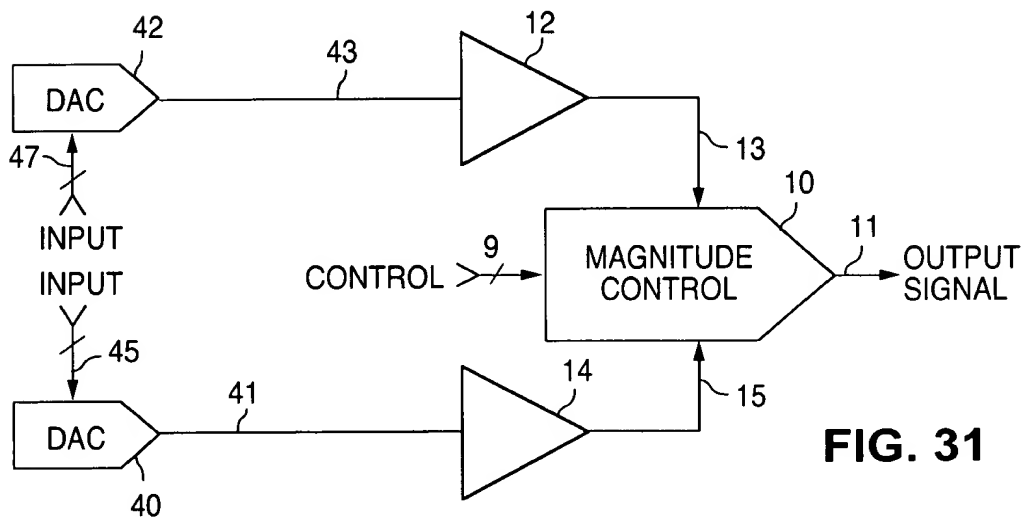


FIG. 31

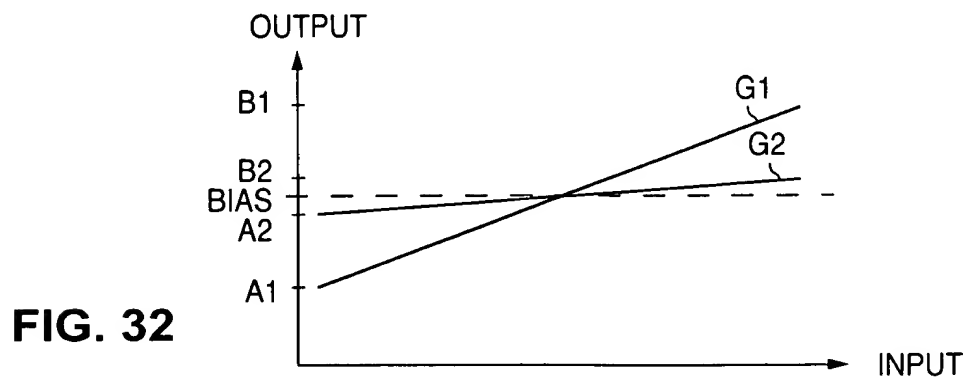


FIG. 32

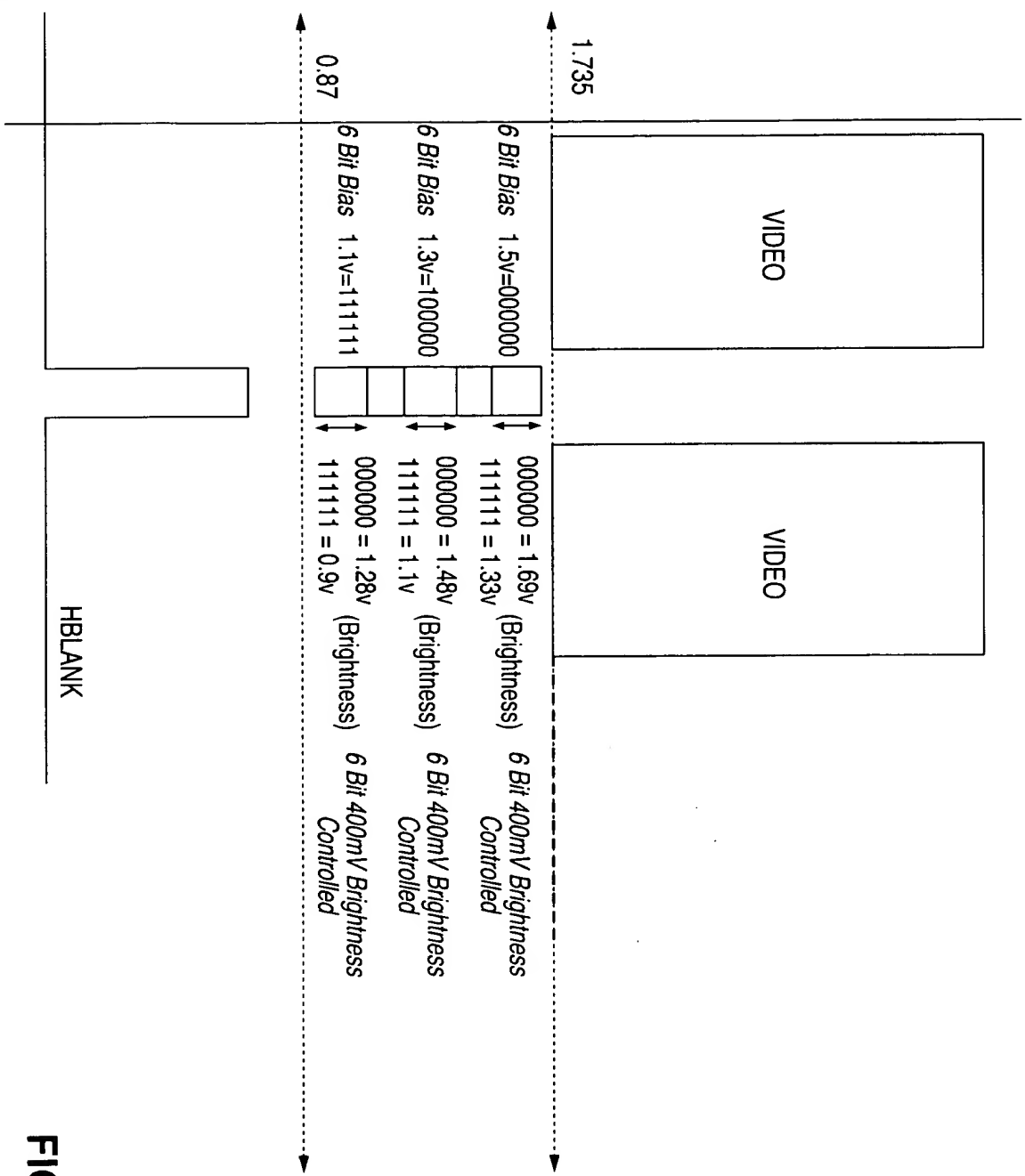


FIG. 33

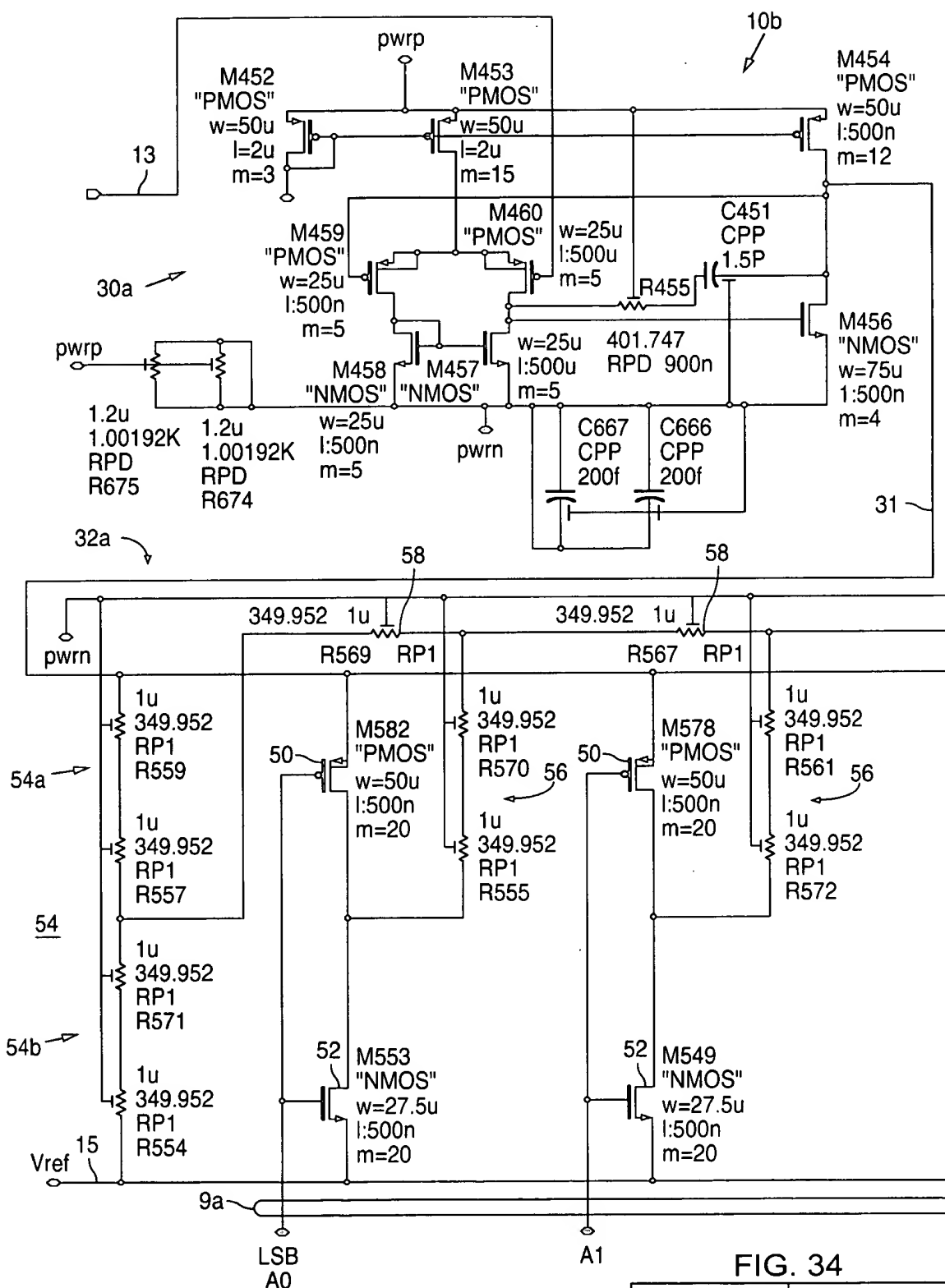


FIG. 34A

FIG. 34

FIG. 34A	FIG. 34B
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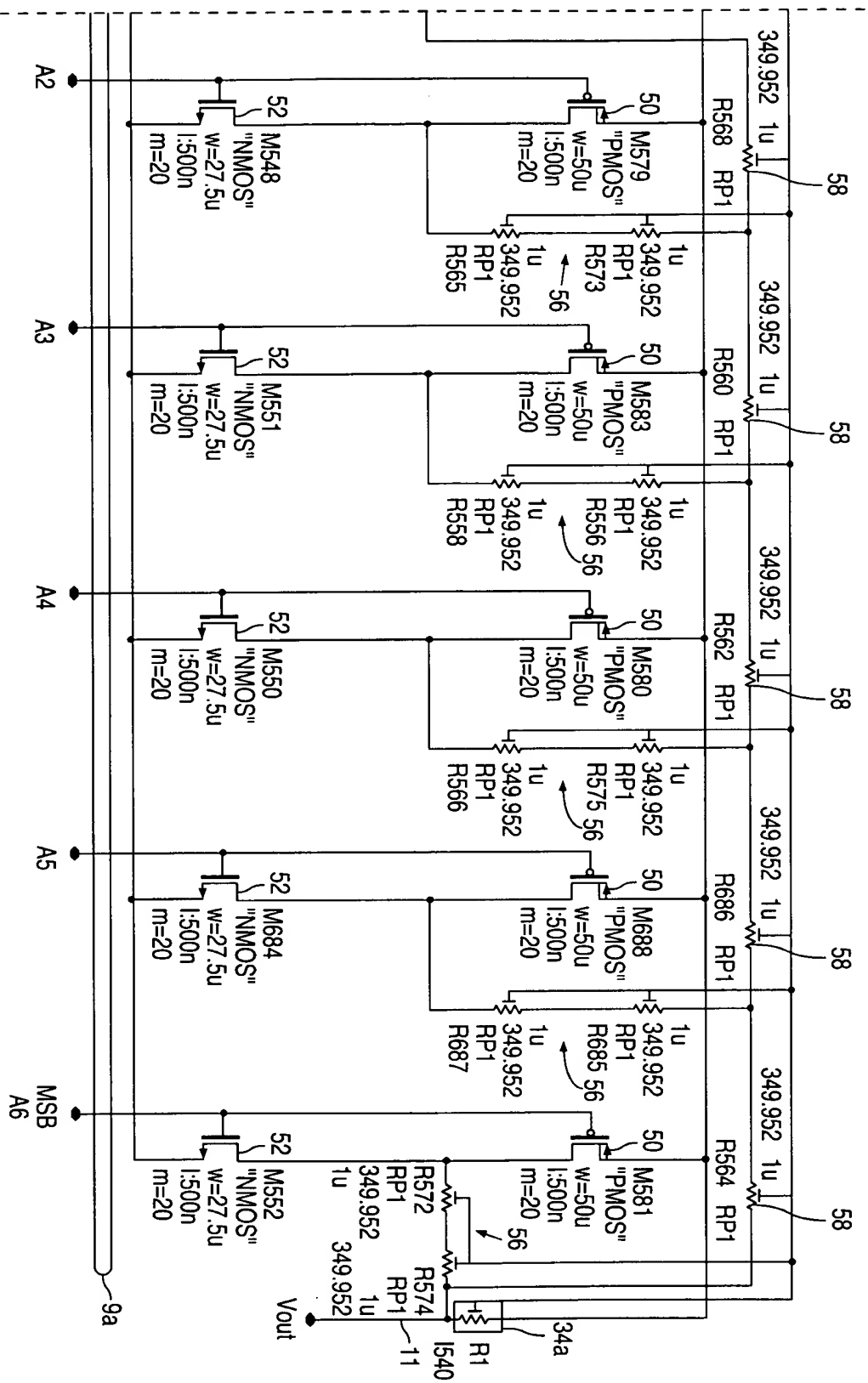


FIG. 34B



FIG. 35A

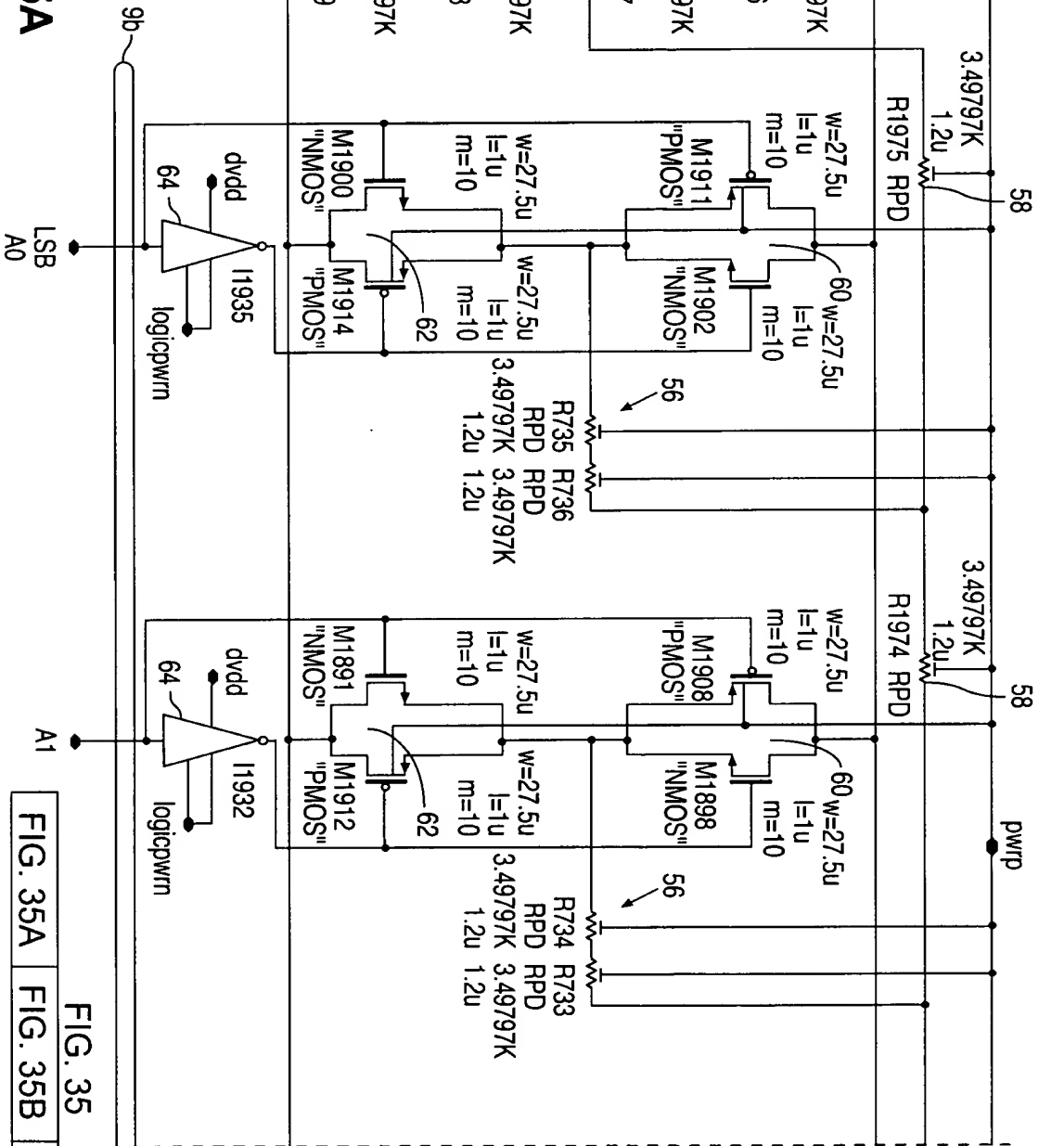


FIG. 35A

FIG. 35B

FIG. 35C

FIG. 35

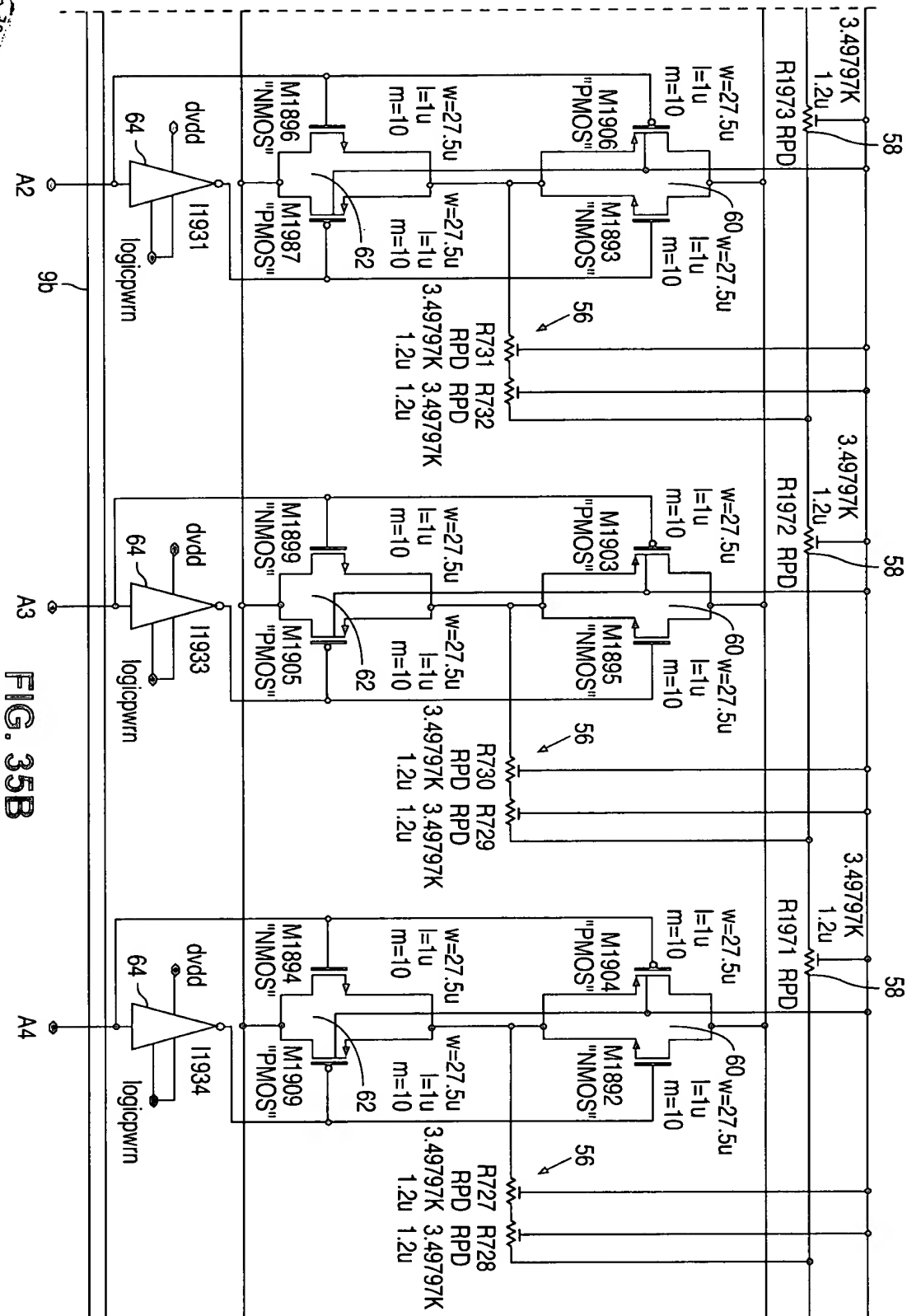


FIG. 35

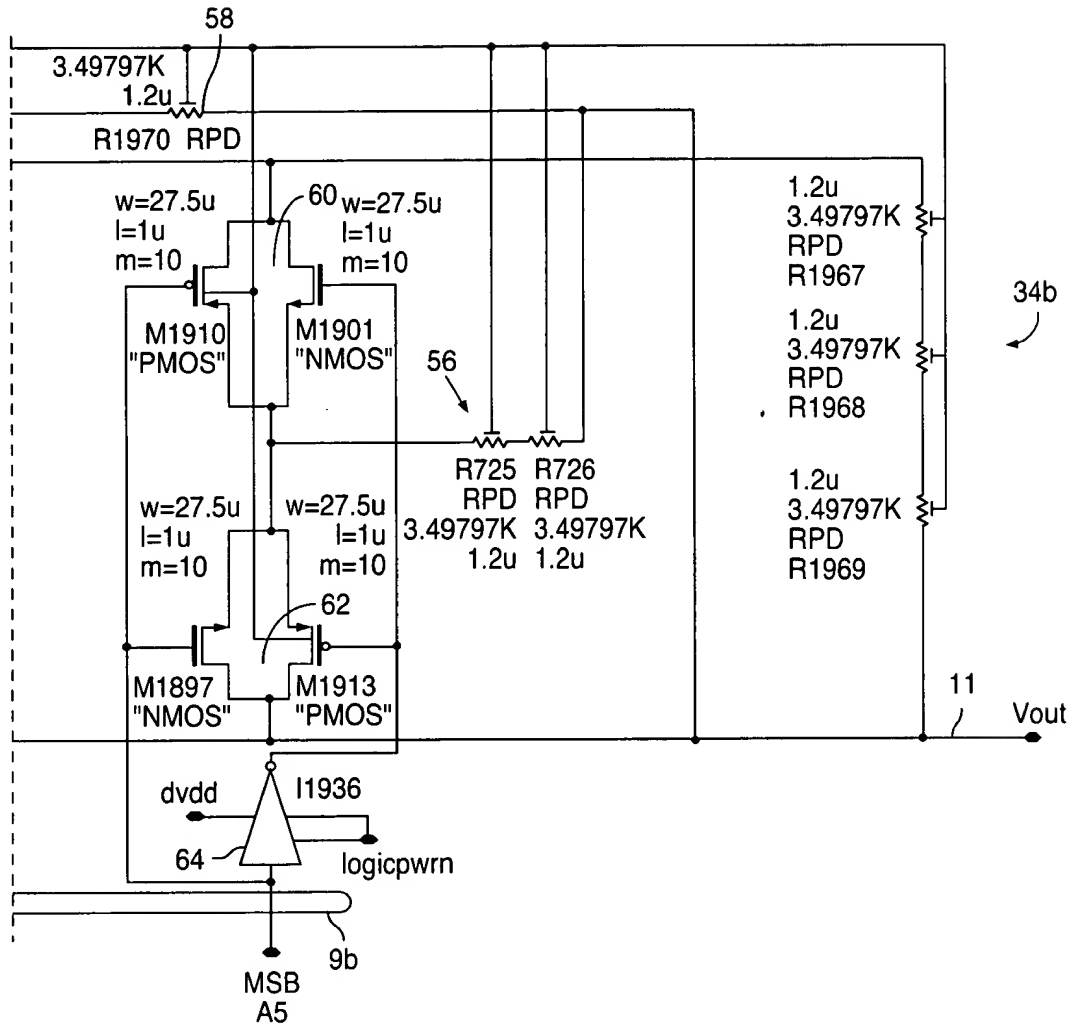


FIG. 35C

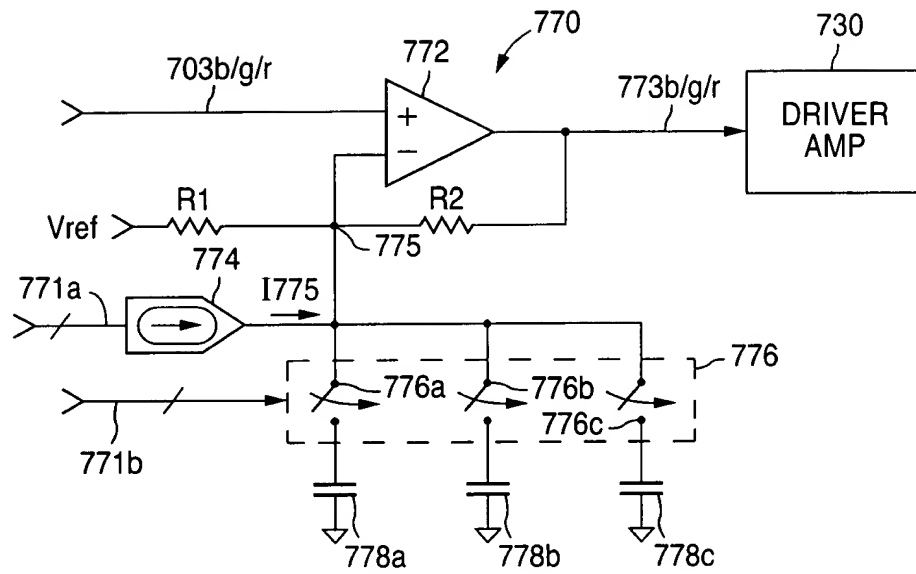


FIG. 36

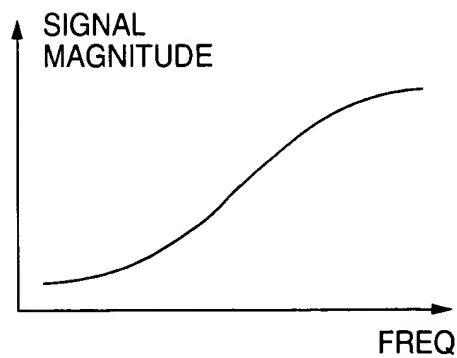


FIG. 37

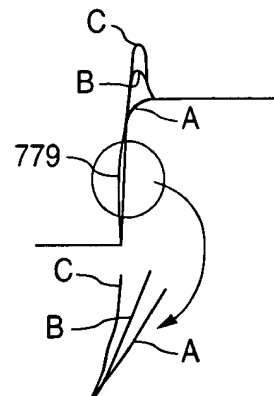


FIG. 38